Digital Design

CSCE 2114-L007

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Introduction

The purpose of this lab was a lot like the purpose of the previous lab where VHDL code had to be written from scratch. The only difference is that the code had to be written to implement a Moore type state machine and since VHDL code had been written in the previous lab this lab was not unfamiliar territory like the previous lab was.

Design

Since the previous lab dealt with writing VHDL code, that made this lab much easier to accomplish. The Moore type state machine that this lab used implements a 2-bit up counter, count, as the output with clock (CLK), reset (Rstn), and enable as inputs. The counter, which is 2-bits, has 2 values and anytime the Rstn and Enable are both active high then the counter will continue to count from 00 to 11 over and over again. If Rstn is ever low then the counter will be forced to 00 and will stay at 00 regardless of the other inputs until it is active high. The counter is only enabled when Enable is an active high and if Enable is ever active low it will stop the counter unless the aforementioned Rstn is ever low then the counter goes to 00. Below is a copy of the VHDL code written for this assignment.

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

ENTITY lab8 IS

PORT( Clock, Rstn, Enable :IN STD\_LOGIC;

Count :OUT STD\_LOGIC\_VECTOR(1 DOWNTO 0));

END lab8;

ARCHITECTURE Behavior OF lab8 IS

TYPE State\_type IS(A,B,C,D);

SIGNAL y : State\_type;

BEGIN

PROCESS(Rstn,Clock)

BEGIN

IF Rstn ='0' THEN

Count <= "00";

y <= A;

ELSIF (Clock'EVENT AND Clock = '1') THEN

CASE y IS

WHEN A=>

IF Enable = '0' THEN

Count <= "00";

y <= A;

ELSE

Count <= "01";

y <= B;

END IF;

WHEN B=>

IF Enable = '0' THEN

Count <= "01";

y <= B;

ELSE

Count <= "10";

y <= C;

END IF;

WHEN C=>

IF Enable = '0' THEN

Count <= "10";

y <= C;

ELSE

Count <= "11";

y <= D;

END IF;

WHEN D=>

IF Enable = '0' THEN

Count <= "11";

y <= D;

ELSE

Count <= "00";

y <= A;

END IF;

END CASE;

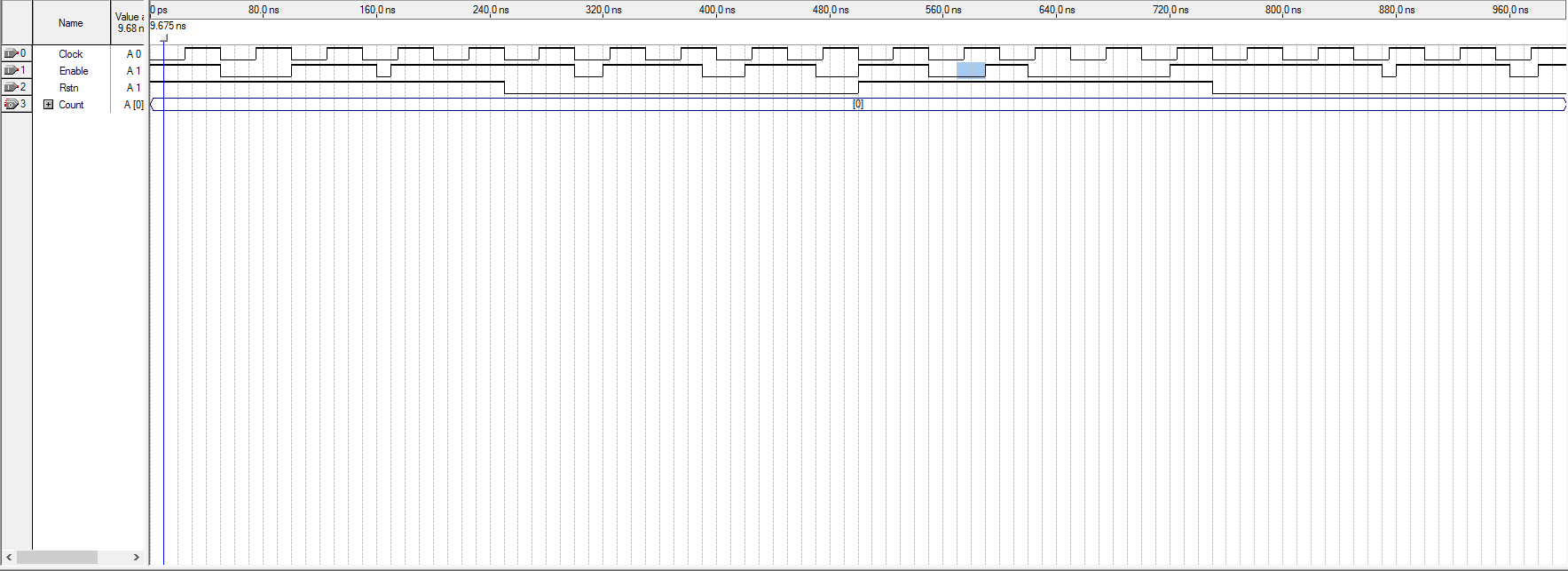
END IF;

END PROCESS;

END Behavior;

Results

The results for VHDL code is shown in a vector waveform graph below. As the results show. Whenever Rstn and Enable are both active high the counter will count from 00 to 11 endlessly and it is only when Enable is active low that the counter stops and whenever Rstn is active low to counter resets to 00. Clock is unaffected by any changes made in Enable or Rstn.



Conclusion

With this being the second lab having to deal with writing VHDL code from scratch it was much easier to complete since being introduced to it in the last lab. One thing that also made this lab easier was drawing out the Moore type state machine on paper and then referring to the VHDL code in the lecture notes on how to properly write the code to implement the Moore type state machine.